EXHIBIT 1

TABLE 1

COMPARISON OF *OKAWA* AND CLAIM 1 OF THE '002 PATENT

Claim 1	*Okawa*
1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:	*Okawa* teaches a method for the prevention of electrostatic destruction of "active matrix display apparatus." (Trial Slide 146); (Trial Tr. 1611:23-1613:7; 1615:13-1616:14; *Okawa* p. 2; *see* Title of the Invention, Claims, Detailed Description of Invention, Field of Industrial Use.)
providing a substrate;	*Okawa* uses "a substrate on which active components and the like are formed." (Trial Tr. 1616:16-1617:10; *Okawa* p. 3.)
forming a pattern of pixels on said substrate;	*Okawa* forms pixels using rows and columns. (Trial Tr. 1617:11-23; *Okawa* p. 4, Fig. 1.)
forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;	*Okawa* forms "a plurality of row and column intersecting pixel activation lines." (Trial Tr. 1617:24-1618:7; *Okawa* p. 4, Fig. 1.) The *Okawa* method calls for connection of individual row or column lines to the outer guard ring via diodes. (Trial Tr. 1618:8-22; *Okawa* p. 5, Fig. 2; p. 2, Overview.)
forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and	*Okawa* teaches forming an outer ESD guard ring, which it calls "short-circuit bus" or S_B. (Trial Tr. 1618:23-1619:15; *Okawa* p. 5, Fig. 2; p. 3, Means for Solving the Problems.) *Okawa*'s method couples individual row and column lines to the outer ring via diodes. (Trial Tr. 1614:8-1615:12; 1618:23-1619:15; *Okawa* p. 5, Fig. 2; p. 2, Overview.) According to the jury, a diode is equivalent to "a resistance." Therefore, *Okawa* teaches this element.
removing said outer guard ring and row and column interconnections prior to completion of the display.	As explained by Dr. Howard, the short-circuit bus in *Okawa* is removable and used during the manufacturing process. (Trial Tr. 1619:17-162.) The *Okawa* guard ring is an improvement over an earlier guard ring that "is removed after the

Claim 1	*Okawa*
	manufacturing process is completed." (*See Okawa*, p. 2, Prior Art.) The improvement of *Okawa* over the prior art is to replace direct shorts with diodes so that each gate or source line can be individually tested "during the manufacturing process." (*See Okawa* pp. 3-4.) Thus, to a person of ordinary skill in the art, the guard ring of *Okawa* must be removable like the prior art upon which it improves. (Trial Tr. 1619:17-1621:9.) The design of the *Okawa* guard ring reflects its removable nature. The source and gate lines are essentially coupled together via symmetric nonlinear diodes. (*See Okawa* Fig. 1.) As explained by the *Okawa* reference itself, these diodes have a "breakdown voltage ... set to be sufficiently lower than the dielectric breakdown voltage across the gate and the drain but sufficiently high enough for measurement of the properties." (*See Okawa* p. 3.) Thus, the guard ring connection in *Okawa* is only designed to handle small testing voltages. If such a guard ring is not removed prior to the completion of the display, it might limit the larger gate signals and thus affect the performance of the LCD panels. (Trial Tr. 1621:10-25.)

EXHIBIT 2

TABLE 2

COMPARISON OF *KAWAMURA* AND CLAIM 1 OF THE '002 PATENT

Claim 1	Kawamura
1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:	*Kawamura* teaches a "method for the manufacture of an active matrix driven apparatus." (Trial Tr. 1627:20-1628:9; Kawamura p. 3; Claim 1.)
providing a substrate;	*Kawamura* uses "active matrix array substrate." (Trial Tr. 1630:23-1631:5; Kawamura p. 3; p. 2, claim 1.)
forming a pattern of pixels on said substrate;	*Kawamura* forms pixels using rows and columns. (Trial Tr. 1631:6-12; Kawamura p. 11, Fig. 1.)
forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;	*Kawamura* forms "a plurality of first wirings and a plurality of second wirings which mutually intersect with an insulation layer interposed in between." (Trial Tr. 1631:13-25; Kawamura p. 2, claim 1; p. 11, Fig. 1.) The "first wirings" are row lines. (Kawamura p. 11, Fig. 1, items 101; p. 12, Fig. 3, items 101; p. 12, Fig. 4, item 101.) The "second wirings" are column lines (Kawamura p. 11, Fig. 1, items 102; p. 12, Fig. 3, item 102; p. 12, Fig. 4, item 102; see also p. 6 ("The gate electrodes of the TFTs are connected to the first wirings 101, and the source electrodes are connected to the second wirings 102.").) *Kawamura* teaches a group of third wirings that "connect the ends of the first wirings …so as to form one long electrically connected serpentine wiring." (Trial Tr. 1628:18-1630:14; 1632:1-17; Kawamura p. 5; p. 11, Fig. 1, item 103; p. 12, Fig. 3, item 103; p. 12, Fig. 4, item 103a.) This "serpentine wiring" is formed by connecting the ends of the first wiring (i.e., row lines) "alternately." (Trial Tr. 1628:18-1630:14; 1632:1-17; Kawamura p.6; p. 11, Fig. 1; p. 12, Figs. 3 & 4.) *Kawamura* also teaches similar connections by the "third wirings" for the "second wirings" (i.e., the column lines). (Trial Tr. 1628:18-1630:14; 1632:1-17; Kawamura p. 5; p. 11, Fig. 1, item 103, Fig. 4, item 103a ("The same arrangement is used for the second wiring as for the first wiring").)
forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and	*Kawamura* forms a "fourth wiring," which in one embodiment is a continuous conductor ring. (Kawamura p. 12, Fig. 3, item 300.) It states that "wiring 300 which extend over the entire substrate, thus creating a construction that

Claim 1	Kawamura
column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and	allows an even quicker dispersion of electrostatic charges. (Common electrode wiring 105 may be used as the wiring 300)." (Kawamura p. 8.) Wiring 300 in Kawamura is thus "the outer electrostatic discharge guard ring." (Trial Tr. 1632:18-1633:4.) Kawamura is coupled to the interconnected "first wirings" and "second wirings" through the "fourth wirings" that "use[] ring diodes." (Trial Tr. 1632:18-1633:4; Kawamura p. 7, p. 10, Fig. 2, item 107; p. 11, Fig. 1, items 104 & 107; p. 12, Fig. 3, items 104 & 107; see p. 8 ("With this embodiment, the first wirings 101 and the second wirings 102 are connected by means of the fourth wirings 104 disposed with ring diodes and by wiring 300.").) According to the jury, a diode is equivalent to "a resistance." Therefore, Kawamura teaches this element.
removing said outer guard ring and row and column interconnections prior to completion of the display.	Kawamura teaches removing the interconnections and outer guard ring through etching. (Trial Tr. 1628:11-15; 1633:5-1634:2; Kawamura pp. 6-8; Figs. 1-3, item 106; p. 6 ("... the electrostatic countermeasures can be removed relatively easily by an etching process at any point in time"); p. 7 ("the electrical short-cuts established by the third and the fourth wirings as countermeasures against static electricity can be removed at any point in time by etching ...").)

EXHIBIT 3

TABLE 3

COMPARISON OF *ORITSUKE* AND CLAIM 8 OF THE '002 PATENT

Claim 8	*Oritsuke*
8. The method as defined in claim 1;	As explained above, *Kawamura* and *Okawa* teach the method defined in claim 1. *Oritsuke* teaches a method of manufacturing "flat displays such as liquid crystal displays," especially "active matrix flat displays" in which an inner ESD guard ring is used. (*Oritsuke* p. 3; p. 4; p. 7, Fig. 1.)
including forming an inner electrostatic discharge guard ring on said substrate	*Oritsuke* forms an inner electrostatic discharge guard ring called "ground line E." (p. 4; p. 7, Fig. 1.) The display is made on top of "a glass substrate SUB." (*Oritsuke* p. 5 ("patterned on a glass substrate SUB"); p. 8, Fig. 4).)
coupled to said row and column lines via shunt switching elements to provide protection for electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.	*Oritsuke* forms a pattern of pixels on the substrate. (*Oritsuke*, p. 4 ("A panel PNL of a liquid crystal display apparatus LCD comprises a plurality of pixels PIX connected in a matrix between scan lines X and signal lines Y"); p. 7, Fig. 1.) *Oritsuke* forms a plurality of row and column intersection pixel activation lines. (*Oritsuke* p. 4; p. 7, Fig. 1.) *Oritsuke* forms an inner electrostatic discharge guard ring called "ground line E." (*Oritsuke* p. 4; p. 7, Fig. 1.) Ground line E is coupled to the row and column lines via shunt switching elements ("protective transistors") (*Oritsuke* p. 4; TFT1 and TFT2 in Fig. 1, or TFT1, TFT2, TFT3, and TFT4 in Fig. 5, or TFT1, TFT2, TFT5, and TFT6 in Fig. 6.) This inner guard ring and its shunt switching elements provide protection from electrostatic discharges during the manufacture of the displays and thereafter. The invention was designed to solve the problem of "the destruction or the deterioration in the performance of the active components 4 by static electricity created during the [manufacturing] process or during installation to or removal from a panel." (*Oritsuke* p. 4.)

EXHIBIT 4

TABLE 4

COMPARISON OF *YUDASAKA* AND CLAIM 8 OF THE '002 PATENT

Claim 8	*Yudasaka*
8. The method as defined in claim 1;	As explained above, *Kawamura* and *Okawa* teach the method defined in claim 1. *Yudasaka* teaches a method of manufacturing "active matrix 7 comprising TFTs (thin film transistors)," and especially a method for protecting the TFTs from electrostatic discharge damages, using an inner ESD guard ring. (*Yudasaka* p. 2.)
including forming an inner electrostatic discharge guard ring on said substrate	The "transistors are formed on an insulating substrate." (*Yudasaka* p. 2.) *Yudasaka* forms a pattern of pixels on the substrate. (*Yudasaka* p. 4; p. 5, Figs. 1 & 2.) *Yudasaka* forms an inner electrostatic discharge guard ring called "wiring A." (*Yudasaka* p. 3; p. 5, Fig. 2.)
coupled to said row and column lines via shunt switching elements to provide protection for electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.	*Yudasaka* forms an inner electrostatic discharge guard ring called "wiring A." (*Yudasaka* p. 3; p. 5, Fig. 2.) Wiring A is coupled to the row and column lines via pairs of MOS transistors. (*Yudasaka* p. 3; p. 5, Fig. 2.) This inner guard ring and its shunt switching elements ("MOS transistors") provide protection from electrostatic discharges during the manufacture of the displays and thereafter. (*Yudasaka* p. 3 ("During the manufacturing process ... wiring A is in a floating state ...."); p. 3 ("When the assembly of the active matrix is completed ...it is preferable to connect wiring A to a ground potential as well. The protection circuit according to the present invention will then work not only against electrostatic charges but also against surges that enter through the peripheral circuits.").)